APEC 2024 Industry Session Proposal

Power Electronics for High Performance Computing: New Opportunities and Challenges Since 2022

Panelists and Speakers (1 Host + 6 Speakers)

- **Minjie Chen**, Princeton University (Host)
- **Robert Pilawa-Podgurski**, UC Berkeley
- **Kaladhar Radhakrishnan**, Intel
- **Shuai Jiang**, Google
- **Sudhir Kudva**, Nvidia
- **Shenggao Li**, TSMC
- **Jeffrey Morroni**, Texas Instruments

Preliminary Session Schedule (120 min)

Session Overview (15 min):

Power electronics for high-performance computing: technology overview

- **Minjie Chen**, Princeton University

Technical Presentations (6 x 15 min):

Recent Advances in IVR Solutions for High Power Microprocessors

- **Kaladhar Radhakrishnan**, Intel

Challenges to enabling Vertical power delivery in high-power GPU applications

- **Sudhir Kudva**, Nvidia

Multi-MHz Bandwidth TLVR and Power Delivery for Next-Generation AI Systems

- **Shuai Jiang**, Google

Finding the best topology for the job: Quantitative methods for evaluating performance of hybrid switched-capacitor dc-dc converter topologies for data center applications

- **Robert Pilawa-Podgurski**, UC Berkeley

Title: The Role of Passive Integration in Future VR Solutions

- **Jeffrey Morroni**, Texas Instruments

Power Delivery for High-speed Die to Die Interconnects and future 3D-ICs

- **Shenggao Li**, TSMC

Session Summary

We have organized a very successful industry session “Power Electronics for High Performance Computing: Opportunities and Challenges” in APEC 2022. This is a rapidly evolving area. We hope to revisit this topic after 2 years and discuss the new opportunities and challenges.

U.S. data centers currently consume more than 90 billion kilowatt-hours of electricity a year and produce as much CO2 emission as the entire airline industry. Traditional power delivery architectures in data centers are bulky and inefficient. Only 60% of electricity is used for computing and the rest is lost in the power conversion process. Advanced power electronics systems are needed to support the future development of high-performance computing and telecommunication infrastructures.

Future microprocessors comprise billions of transistors, switch at a few GHz, and each consumes hundreds of amperes of current at very low voltage (i.e., <0.8V). Delivering hundreds of watts of power with stability and fast control while maintaining high efficiency are major obstacles for future Point-of-Load (PoL) converters. High performance computing (such as machine learning) is usually closely connected with “Big Data”. Advanced power electronics architecture which can efficiently support large-scale data storage opens a wide range of opportunities. For data centers, high voltage dc power delivery, advanced grid interface, and the possibility of powering high performance computing with renewable energy brings new challenges to power electronics.

We have assembled a panel with experts from academia and industry with extensive experience in semiconductor devices, magnetics, circuit topologies, and system architectures to discuss the future research opportunities in power electronics for high performance computing with ultra-high efficiency and unprecedented functionality.

Prof. Minjie Chen (Princeton) will start the session with a 15-min overview. **Dr. Kaladhar Radhakrishnan (Intel)** will provide an overview of recent advances in IVR solutions for high power microprocessors. **Dr. Sudhir Kudva (Nvidia)** will talk about the challenges to enabling vertical power delivery for high current GPUs**. Dr. Shuai Jiang (Google)** will discuss the challenges and opportunities for high frequency TLVR design and control. **Prof. Robert Pilawa (UC Berkeley)** will provide a comprehensive overview of topology selection methods for high performance computing applications. **Dr. Jeffrey Morroni (Texas Instruments)** will talk about the Role of Passive Integration in Future VR Solutions. **Dr. Shenggao Li (TSMC)** will talk about Power Delivery for High-speed Die to Die Interconnects and future 3D-ICs**.**